+3 Volt, Dual, Serial-Input 12-/10-Bit DAC

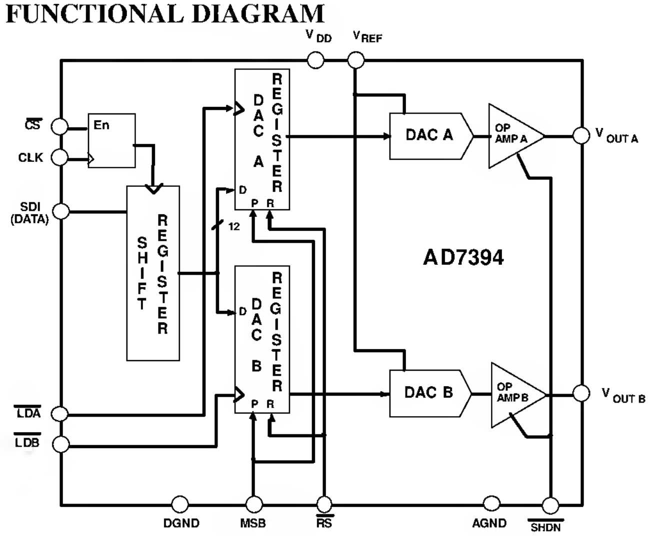
Preliminary

AD7394/AD7395

FEATURES
Micro Power - 100µA/DAC
0.1µA Typical Power Shutdown
Single-Supply +2.7 to +5.5 Volt Operation
Compact 1.1mm Height TSSOP-14 Package
AD7394 – 12-bit Resolution
AD7395 – 10-bit Resolution
3-wire serial SPI Compatible Interface with Schmitt Trigger Inputs
0.9 LSB Differential Nonlinearity Error

APPLICATIONS
Automotive 0.5 to 4.5V Output Span Voltage
Portable Communications
Digitally Controlled Calibration
PC Peripherals

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The AD7394/95 family of dual, 12-/10-bit, voltage-output digital-to-analog converters are designed to operate from a single +3 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in single-supply +3 volt systems. Operation is guaranteed over the supply voltage range of +2.7 to +5.5V making this device ideal for battery operated applications.

The Full-Scale output voltage is determined by the applied external reference input voltage VREF. The rail-to-rail VREF input to V_{OUT} outputs allow for a Full-Scale voltage set equal the positive supply V_{DD} or any value in between.

A doubled-buffered serial-data interface offers high-speed, three-wire, SPI and microcontroller compatible inputs using serial-data-in (SDI), clock (CLK) and load strobe (LDA+LDB) pins. A chip-select (CS) pin simplifies connection of multiple DAC packages by enabling the clock input when active low.

Additionally, a RS input sets the output to zero scale or to 1/2 scale based on the logic level applied to the MSB pin. The power shutdown pin SHDN reduces power dissipation to nanoamp current levels. All digital inputs contain Schmitt triggered logic levels to minimize power dissipation and prevent false triggering on the clock input.

Both parts are offered in the same pin out to allow the user to select the amount of resolution appropriate for their application without circuit card redesign.

The AD7394/AD7395 are specified over the extended industrial (-40°C to +85°C) temperature range. Packages available include plastic DIP, and low profile 1.75 mm height SO-14 surface mount packages. The AD7395ARU is available for ultra compact applications in a thin 1.1 mm TSSOP-14 package. For automotive applications the AD7395AR is specified for operation over the (-40°C to +125°C) temperature range.

PRELIMINARY REV 0.12, 16FEB97

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AD7394 12-Bit Rail-to-Rail Voltage Out DAC

ELECTRICAL CHARACTERISTICS at V_{REF}in = 2.5V, -40°C < T_A < +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	3V±10%	5V±10%	UNITS
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.5	±1.5	LSB max
Relative Accuracy[2]	INL	T_A = -40°C, +85°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	T_A = 25°C, Monotonic	±0.9	±0.9	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	4.0	4.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, Data = FFF_H	±8	±8	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = -40°C, Data = FFF_H	±20	±20	mVmax
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
V_{REF}in Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5LSB	1	1	mA typ
Output Current (sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD}-0.6	V_{DD}-0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3,5]					
Clock Width High	t_{CH}		50	30	ns min
Clock Width Low	t_{CL}		50	30	ns min
Load Pulse Width	t_{LDW}		30	20	ns min
Data Setup	t_{DS}		10	10	ns min
Data Hold	t_{DH}		30	15	ns min
Clear Pulse Width	t_{CLRW}		15	15	ns min
Load Setup	t_{LD1}		30	15	ns min
Load Hold	t_{LD2}		40	20	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5V_{DC} +1V_{P-P}, Data = 000_H, f=100KHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL<±1LSB	2.7/5.5	2.7/5.5	V min/max
Shutdown Supply Current	I_{DD_SD}	SHDN=0, V_{IL} = 0V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0V, No Load	--/200	--/200	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0V, No Load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.003	0.006	%/% max

NOTES:

1. One LSB = V_{REF}/4096V for the 12-bit AD7394.
2. The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
3. These parameters are guaranteed by design and not subject to production testing.
4. Typicals represent average readings measured at 25°C.
5. All input control signals are specified with t_R = t_F = 2ns (10% to 90% of +3V) and timed from a voltage level of 1.6V.
6. The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

AD7395 10-Bit Rail-to-Rail Voltage Out DAC

ELECTRICAL CHARACTERISTICS at V_{REF}in = 2.5V, -40°C < T_A < +85°C/+125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	3V±10%	5V±10%	UNITS
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.5	±1.5	LSB max
Relative Accuracy[2]	INL	T_A = -40°C, 85°C, 125°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±0.9	±0.9	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, 125°C, Data = $3FF_H$	±32	±32	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = -40°C, Data = $3FF_H$	±35	±35	mV max
Full-Scale Tempco[3]	TCV_{FS}		16	16	ppm/°C typ
REFERENCE INPUT					
V_{REF}in Range	V_{REF}		$0/V_{DD}$	$0/V_{DD}$	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[1]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (source)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5LSB	1	1	mA typ
Output Current (sink)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V min
Logic Input High Voltage	V_{IH}		V_{DD}-0.6	V_{DD}-0.6	V max
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3,5]					
Clock Width High	t_{CH}		50	30	ns
Clock Width Low	t_{CL}		50	30	ns
Load Pulse Width	t_{LDW}		30	20	ns
Data Setup	t_{DS}		10	10	ns
Data Hold	t_{DH}		30	15	ns
Clear Pulse Width	t_{CLRW}		15	15	ns
Load Setup	t_{LD1}		30	15	ns
Load Hold	t_{LD2}		40	20	ns
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	$V_{REF} = 1.5V_{DC} + 1V_{P-P}$, Data = 000_H, f=100KHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL<±1LSB	2.7/5.5	2.7/5.5	V min/max
Shutdown Supply Current	I_{DD_SD}	SHDN=0, V_{IL} = 0V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0V, No Load	--/200	--/200	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.003	0.006	%/% max

NOTES:
1. One LSB = V_{REF}/1024V for the 10-bit AD7395.
2. The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
3. These parameters are guaranteed by design and not subject to production testing.
4. Typicals represent average readings measured at 25°C.
5. All input control signals are specified with $t_R = t_F$ = 2ns (10% to 90% of +3V) and timed from a voltage level of 1.6V.
6. The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

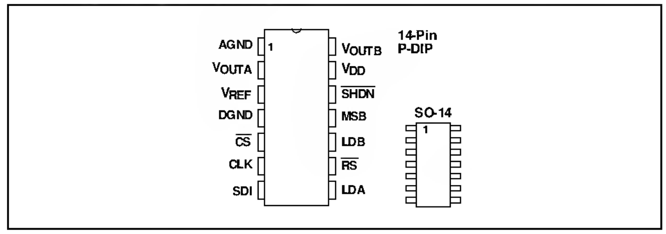
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... –0.3V, +7V
VREF to GND .... –0.3V, V_{DD}
Logic Inputs to GND .... –0.3V, +8V
V_{OUT} to GND .... –0.3V, V_{DD} + 0.3V
I_{OUT} Short Circuit to GND 50mA
Package Power Dissipation .... $(T_J\,MAX - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
  14-Pin Plastic DIP Package (N-14) .... 103°C/W
  14-Lead SOIC Package (R-14) .... 158°C/W
  14-lead Thin Shrink Surface Mount (RU-14) .... 180°C/W
Maximum Junction Temperature (T_J MAX) .... 150°C
Operating Temperature Range .... –40°C to +85°C
  AD7495AR only .... –40°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature:
  N-14 (Soldering, 10 secs) .... +300°C
  R-14 (Vapor Phase, 60 secs) .... +215°C
  RU-14 (Infrared, 15 secs) .... +224°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE:

MODEL	RES	TEMP RANGE	Package Description	Package Option
AD7394AN	12	-40/+85°C	14-pin P-DIP	N-14
AD7394AR	12	-40/+85°C	14-lead SOIC	R-14
AD7395AN	10	-40/+85°C	14-pin P-DIP	N-14
AD7395AR	10	-40/+125°C	14-lead SOIC	R-14
AD7395ARU	10	-40/+85°C	TSSOP-14	RU-14

The AD7394/95 contains 700 transistors. The die size measures 70 mil X 99 mil.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7394/95 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

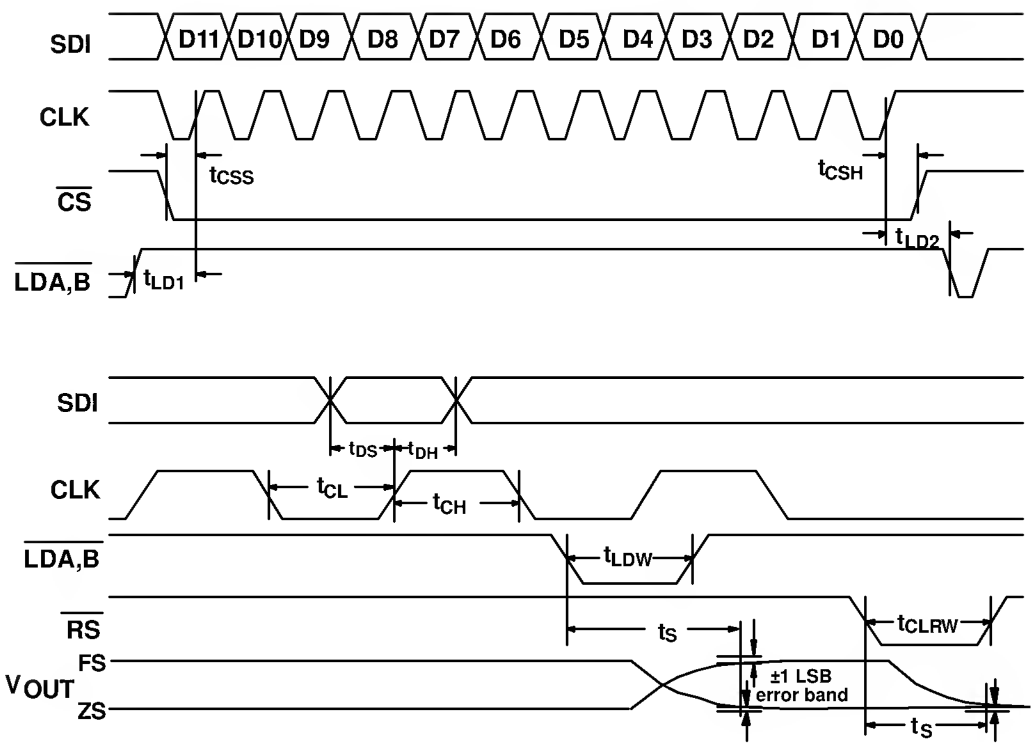


Figure 3A Timing Diagram

Figure 3B Timing Diagram

Table 1. Control-Logic Truth Table

CS	CLK	RS	MSB	SHDN	LDA/B	Serial Shift Register Function	DAC Register Function
H	X	H	X	H	H	No Affect	Latched
L	L	H	X	H	H	No Affect	Latched
L	H	H	X	H	H	No Affect	Latched
L	↑+	H	X	H	H	Shift-Register-Data advanced one bit	Latched
↑+	L	H	X	H	H	No Affect	Latched
H	X	H	X	H	↓–	No Affect	Updated with current Shift Register contents
H	X	H	X	H	L	No Affect	Transparent
X	X	L	H	H	X	No Affect	Loaded with 800_H
X	X	↑+	H	H	H	No Affect	Latched with 800_H
X	X	L	L	H	X	No Affect	Loaded with all zeros
X	X	↑+	X	H	H	No Affect	Latched all zeros
X	X	X	X	L	X	No Affect	No Affect

Notes:
1. ↑+ positive logic transition; ↓– negative logic transition; X Don't Care
2. Do not clock in serial data while level sensitive inputs LDA or LDB are logic LOW.

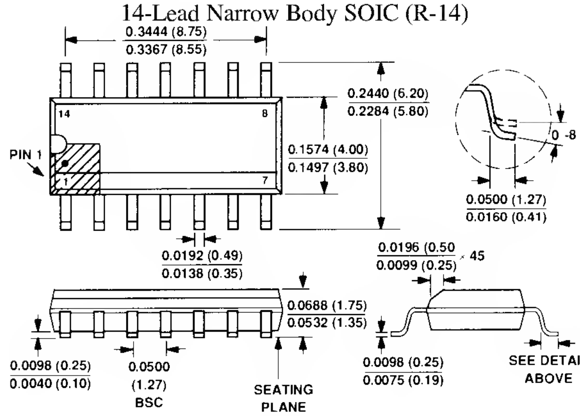
PIN DESCRIPTION

PIN#	Name	Function
1	AGND	Analog Ground.
2	V_{OUTA}	DAC A voltage output.
3	V_{REF}	DAC Reference voltage input terminal. Establishes DAC Full-Scale output voltage. Pin can be tied to V_{DD} pin.
4	DGND	Digital Ground. Should be tied to analog GND
5	CS	Chip Select, active low input. Disables shift register loading when high. Does not effect LDA or LDB operation.
6	CLK	Clock input, positive edge clocks data into shift register.
7	SDI	Serial Data Input, input data loads directly into the shift register.
8	LDA	Load DAC register strobes, level sensitive active low. Transfers shift register data to DAC A register. Asynchronous active low input. See Control Logic Truth Table for operation.
9	RS	Resets DAC register to zero condition or half-scale depending on MSB pin logic level. Asynchronous active low input.
10	LDB	Load DAC register strobes, level sensitive active low. Transfers shift register data to DAC B register. Asynchronous active low input. See Control Logic Truth Table for operation.
11	MSB	Digital Input: Logic High presets DAC registers to half-scale 800_H (sets MSB bit to one) when the RS pin is strobed; Logic Low clears all DAC registers to zero (000_H) when the RS pin is strobed.
12	SHDN	Active low shutdown control input. Does not effect register contents as long as power is present on V_{DD}. New data can be loaded into the shift register and DAC register during shutdown. When device is powered up the most recent data loaded into the DAC register will control the DAC output.
13	V_{DD}	Positive power supply input. Specified range of operation +2.7 to +5.5V
14	V_{OUTB}	DAC B voltage output.

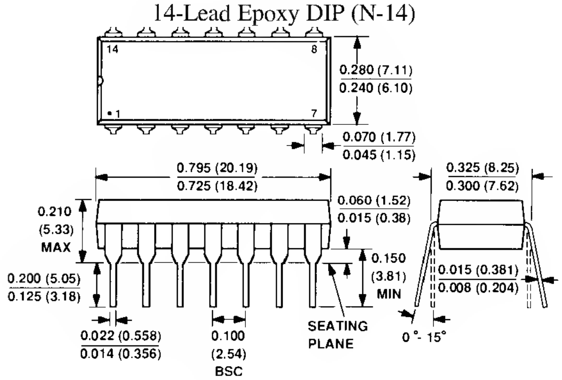
Mechanical Outline Dimensions

Dimensions shown in inches and (mm).

14-Lead Narrow Body SOIC (R-14)



14-Lead Epoxy DIP (N-14)



TSSOP-14 (RU-14)